AIP | Applied Physics Letters

Charge trapping instabilities in amorphous siliconsilicon nitride thinfilm transistors

M. J. Powell

Citation: Appl. Phys. Lett. **43**, 597 (1983); doi: 10.1063/1.94399
View online: http://dx.doi.org/10.1063/1.94399
View Table of Contents: http://apl.aip.org/resource/1/APPLAB/v43/i6
Published by the American Institute of Physics.

Charge trapping instabilities in amorphous silicon-silicon nitride thin-film transistors

M. J. Powell
Philips Research Laboratories, Redhill, Surrey, United Kingdom

(Received 2 June 1983; accepted for publication 7 July 1983)

The most important instability mechanism in amorphous silicon-silicon nitride thin-film transistors is charge trapping in the silicon nitride layer, which leads to a threshold voltage shift (ΔV_T). We have measured the time, temperature, and gate voltage dependence of ΔV_T and conclude that the rate limiting process, in the charge transfer from semiconductor to insulator, is the conduction in the nitride by variable-range hopping. The threshold shift (under positive bias) is temperature dependent with an activation energy of 0.3 eV. This activation energy is identified with the mean hop energy required to inject charge deep into the silicon nitride at the low applied fields appropriate to transistor operation.

PACS numbers: 85.30. — z, 73.60. — n

In recent years, thin-film transistors made with hydrogenated amorphous silicon have been receiving widespread attention owing to their promise for applications involving large area integration such as matrix addressing of liquid crystal displays.[1] For these applications, one requires a large area, low-temperature technology compatible with cheap glass substrates. Glow discharge amorphous silicon is well suited to these requirements and transistors have been fabricated with a number of different structures and gate dielectrics. To date, the best dc transistor characteristics have been obtained with amorphous silicon-silicon nitride thin-film transistors in the inverted staggered electrode configuration,[2–5] where the insulator and semiconductor are deposited sequentially using the same glow discharge method.

Apart from the dc characteristics, an important aspect of transistor performance is their stability.[5] This is particularly important where the gate dielectric is plasma silicon nitride, which is well known to have a high density of trap states[6] and hence potentially suffer from charge trapping instabilities. Indeed, silicon nitride is used in metal-nitride-oxide-silicon (MNOS) memory devices utilizing this charge trapping phenomenon.[7] However, the crucial difference with amorphous silicon-silicon nitride thin-film transistors is that these devices operate with relatively low fields in the dielectric, typically $\sim 3\times 10^5$ V cm^{-1}. It is therefore important to measure the magnitude of the charge trapping instability and to understand the mechanisms responsible at the low fields appropriate to device operation.

In an earlier paper, we reported preliminary measurements of the source-drain current decay under positive bias-temperature stress and showed that the decay was entirely due to a threshold voltage shift (ΔV_T) and that the magnitude of the decay was acceptably small under normal operating conditions.[8] We also tentatively assigned the strong temperature dependence of the threshold voltage shift to the temperature-dependent supply of mobile electrons from the semiconductor.

In this letter we report further measurements of the time, temperature, and gate voltage dependence of the threshold voltage shift brought about by bias stress for both positive and negative bias. Consideration of models to account for the strong temperature dependence leads to the conclusion that the rate limiting process is the conduction in the nitride by variable range hopping and not the supply function from the semiconductor.

The bias-stress measurements are performed on test structures with N$^+$ Si substrates as previously reported.[8] In all cases, the bias stress produces a threshold voltage shift (identical to the flatband voltage shift) with negligible change in off-current, prethreshold current or field-effect mobility, consistent with charge trapping in the insulator. Figure 1 shows the time dependence (up to 6×10^4 s) of ΔV_T for $V_G = 12$ V and a 0.5-μm-thick insulator at a number of temperatures, and Fig. 2 shows the temperature and gate voltage dependence of ΔV_T after a fixed stressing time of 6×10^4 s. The magnitude of the threshold voltage shift is smaller for negative bias, but there is a strong temperature dependence for both polarities. The threshold shifts are less than 1 V at room temperature, but this increases to + 7 V for positive bias at 100 °C and − 3 V for negative bias. We now consider possible mechanisms to account for this temperature-dependent charge transfer.

Fowler–Nordheim injection [(2) in Fig. 3], which is

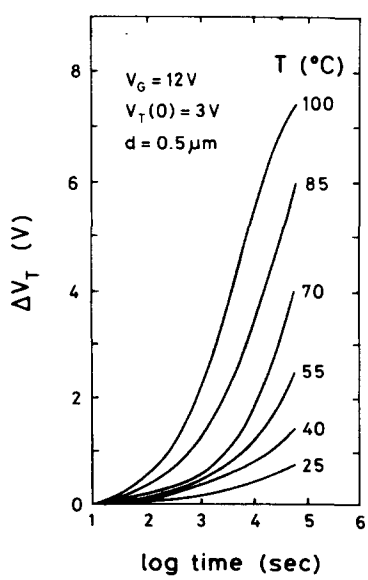

FIG. 1. Time dependence of ΔV_T for a number of different temperatures.

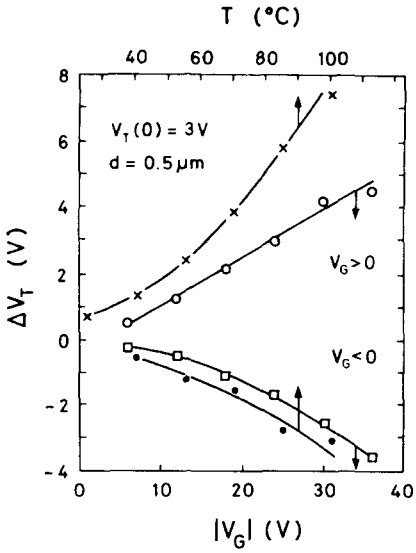

FIG. 2. Threshold voltage shift (after 6×10^4 s) as a function of T ($|V_G| = 12$ V) and V_G ($T = 40$ °C).

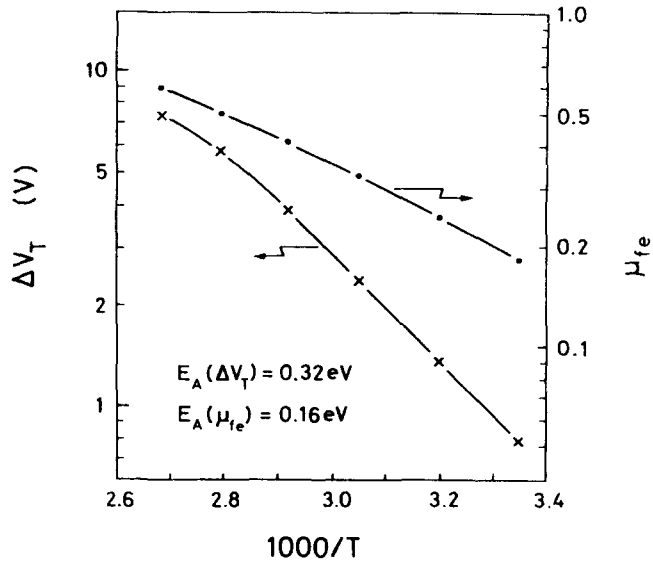

FIG. 4. Temperature dependence of the threshold shift ($V_G = 12$ V, $t = 6\times10^4$ s) and the temperature dependence of the field-effect mobility.

commonly used to account for the writing in MNOS devices,[7,9] can be dismissed since it is limited to high fields. Direct tunneling from the valence band [(1) in Fig. 3] can apparently account for charge transfer at lower fields,[10,11] as can trap-assisted injection [(3) in Fig. 3],[12] but in both cases relatively large fields are still needed to bring empty states at a remote energy within tunneling range, and neither mechanism can account for our results. Direct tunneling from the valence band is also expected to be independent of temperature.[11]

Mechanisms (4) and (5) in Fig. 3 have been used to account for charge trapping in CdSe thin-film transistors (TFT's). Mechanism (5) is the tunneling to states at the Fermi level, either phonon assisted or via surface states, as originally proposed by Koelmans and de Graaf.[13] This model predicts the familiar logarithmic time dependence of the threshold voltage shift.[10]

$$\Delta V_T = r_d \log(1 + t/t_0)\,. \tag{1}$$

The supply function, which may well be temperature dependent, appears in the t_0 term and the constant r_d only contains the density of traps N_t[cm^{-3}] and a tunneling constant λ [cm], both of which are independent of temperature.

For constant energy tunneling, direct from the conduction band [(4) in Fig. 3], Eq. (1) is again obeyed, but the supply function effectively appears in the r_d term.[14] Wright and Anderson[14] used this model to account for the temperature-dependent threshold shift in CdSe TFT's. They found that ΔV_T was thermally activated with an activation energy of 0.1 eV, the same as the field effect mobility (i.e., the supply of mobile electrons). In our case, Fig. 4 shows that the temperature dependence of ΔV_T is not related to the supply of mobile electrons. The activation energy of ΔV_T is 0.32 eV, while that of μ_{fe} is 0.16 eV. However, even if the activation energies were the same, there is a problem with this interpretation. The maximum occupancy of trap states in the insulator is given by their thermal equilibrium occupancy. When the trap states are more than 0.1 eV above E_f, the total density of trap states needs to be unreasonably high to account for the magnitude of ΔV_T.

We propose that the strong temperature dependence observed in our data is due to the subsequent redistribution of charge in the silicon nitride by hopping; i.e., the electrons initially tunnel to states in the nitride, via mechanism (5) in Fig. 3, but after a certain time, when states are filled to a depth x_0, it becomes more favorable for electrons to hop from occupied states at $x < x_0$ to $x > x_0$, rather than these latter states being filled by direct tunneling from the silicon [mechanism (6) in Fig. 3]. The threshold shift per decade of time, according to Eq. (1), is so low that ΔV_T is dominated by the conduction in the nitride and the direct tunneling is limited to a range of time and temperature that is not observed. It is interesting that in the original work of Koelmans and de Graaf,[14] although their data fitted Eq. (1) and was

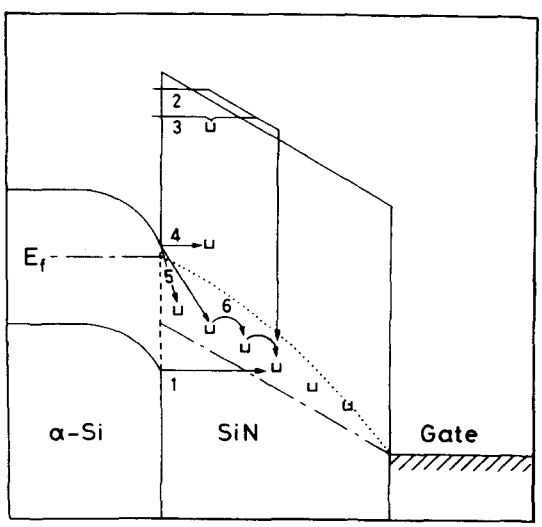

FIG. 3. Charge trapping mechanisms: 1—direct tunneling from valence band; 2—Fowler–Nordheim injection; 3—trap-assisted injection; 4—constant energy tunneling from conduction band; 5—tunneling from conduction band to E_f (phonon assisted or via surface states); 6—hopping at the Fermi level. Chain line—quasi-Fermi level at $t = 0$; dotted line—quasi-Fermi level at $t = \infty$.

essentially temperature independent below room temperature, above room temperature the threshold shift increased with temperature and the time dependence was not simply logarithmic. This is most likely due to a similar mechanism, dominating at the higher temperatures.

An analogous situation is found with charge retention in MNOS devices, which shows an increasing threshold shift at increasing temperatures, which is also due to conduction in the nitride.[15,16] In these cases though, the conduction is attributed to Poole–Frenkel conduction (thermal activation to the conduction band) and the activation energy is > 1 eV.

An activation energy of 0.3 eV suggests thermally activated tunneling, i.e., hopping within a band of trap states at least 0.3 eV wide. For a continuum of trap states, the hopping will be variable range rather than nearest neighbor and a mean hop energy of 0.3 eV implies a density of states $\sim 10^{18}$ $\mathrm{cm}^{-3}\,\mathrm{eV}^{-1}$, for $\alpha^{-1} = 6$ Å (Ref. 17), reasonable values for plasma silicon nitride and consistent with the magnitude of ΔV_T (strictly, the temperature dependence should go as $T^{1/4}$ for variable range hopping, but a well defined activation energy will be observed over a narrow temperature range). As time $t \rightarrow \infty$, a steady state should be reached with all traps between the chain and dotted lines in Fig. 3 filled. However, our experiments suggest that this is not achieved even after 6×10^4 s, which is in agreement with the contention of Arnett and Di Maria,[18] that hopping conduction in silicon nitride at low fields, first suggested by Sze,[19] cannot be observed in the steady state.

In conclusion, we find that the magnitude of the threshold voltage instability, at the low fields appropriate to device operation, is determined by conduction in the nitride by variable-range hopping. This implies that ΔV_T is determined by a property of the nitride, namely, the density of states at the Fermi level (around midgap), since both the hopping conduction and the space charge in the nitride depend on the density of these states. Optimization of the nitride deposition conditions could be beneficial in reducing the midgap trap concentration and hence further improving the device stability, provided this does not adversely affect the amorphous silicon or nitride interface.

The author is indebted to B. C. Easton, O. F. Hill, and J. A. Chapman for device fabrication, D. H. Nicholls for automating the transistor measurements, and to J. M. Shannon, J. F. Verweij, E. Arnold, and J. W. Orton for many useful discussions.

[1] A. J. Snell, K. D. Mackenzie, W. E. Spear, P. G. Le Comber, and A. J. Hughes, Appl. Phys. **24**, 357 (1981).
[2] Y. Okubo, T. Nakagiri, Y. Osada, M. Sugata, N. Kitahari, and K. Hatanaka, Society for Information Display International Symposium 1982, Digest of Technical Papers (1982), p. 40.
[3] H. C. Tuan, M. J. Thompson, N. M. Johnson, and R. J. Lujan, IEEE Electron Dev. Lett. **EDL-3**, 357 (1982).
[4] K. D. Mackenzie, A. J. Snell, I. French, P. G. Le Comber, and W. E. Spear, Appl. Phys. **A31**, 87 (1983).
[5] M. J. Powell, in *Conference Proceedings 'Insulating Films on Semiconductors'*, edited by J. Verweij and D. Wolters (North-Holland, Amsterdam, in press).
[6] A. K. Sinha and T. E. Smith, J. Appl. Phys. **49**, 2756 (1978).
[7] J. J. Chang, IEEE Trans. Electron Devices **ED-24**, 511 (1977).
[8] M. J. Powell and D. H. Nicholls, Proc. IEEE Pat. I **130**, 2 (1983).
[9] K. I. Lundstrom and C. M. Svensson, IEEE Trans. Electron Devices **ED-19**, 826 (1972).
[10] A. V. Ferris-Prabhu, IEEE Trans. Electron Devices **ED-24**, 524 (1977).
[11] S. Fujita, M. Nishihara, W-L. Hoi, and A. Sasaki, Jpn. J. Appl. Phys. **20**, 917 (1981); **20**, 1975 (1981).
[12] C. M. Svensson and K. I. Lundstrom, J. Appl. Phys. **44**, 4657 (1973).
[13] H. Koelmans and H. C. de Graaf, Solid State Electron **10**, 997 (1967).
[14] S. W. Wright and J. C. Anderson, Thin Solid Films **62**, 89 (1979).
[15] L. Lundkvist, C. Svensson, and B. Hansson, Solid State Electron **19**, 221 (1976).
[16] R. A. Williams and M. M. Beguwala, IEEE Trans. Electron Devices **ED-25**, 1019 (1978).
[17] N. F. Mott, Philos. Mag. **19**, 835 (1969).
[18] P. C. Arnett and D. J. Di Maria, J. Appl. Phys. **47**, 2092 (1976).
[19] S. M. Sze, J. Appl. Phys. **38**, 2951 (1967).